

Scalable Floating Gate Flash Memory Cell With Engineered Tunnel Dielectric and High-K (Al_2O_3) Interpoly Dielectric.

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INTRODUCTION

Using conventional SiO_2 and composite oxide-nitride-oxide layers, the possibility for reducing the electrical thickness of tunnel and interpoly dielectrics for floating gate Flash memories is very limited [1]. This leads to the impossibility to decrease the write and erase voltages of Flash memories, which is a major burden for Flash memory scaling towards the 45 nm and 32 nm nodes.

Reduction of the (effective) thickness of the interpoly dielectric can be obtained by the use of high-k materials [2], but reducing the effective thickness of the tunnel oxide requires the use of engineered tunneling barriers. Two different theoretical concepts for such engineered barriers have been proposed in literature: the crested barrier [3] and the Variot stack [4][5]. Experimental demonstration in memory cells has been limited to stacks suitable for efficient tunneling in only one direction [6], which is not suitable for NAND-type memory cells that are both erased and programmed by tunneling through the tunnel dielectric. In this work, we demonstrate for the first time the operation of memory cells with a bidirectional engineered tunneling barrier: a triple layer Variot stack (fig. 1 and 2). Furthermore, these memory cells also have an Al_2O_3 interpoly dielectric and achieve 10 years of data retention up to 120°C.

DEVICE FABRICATION

We have manufactured stacked gate memory cells (fig. 3) in a 90 nm Flash memory process. The tunnel dielectric (three-layer Variot stack) is formed by first growing a 2 nm thermal oxide on the p-type silicon substrate. Then, 8 nm Al_2O_3 is deposited on this oxide by ALCVD, followed by a post-deposition anneal in N_2 at 800°C during 1 minute. Finally, the top HTO oxide is deposited followed by floating gate polysilicon deposition, doping and patterning. The interpoly dielectric consists of 1 nm chemical oxide and 8 nm Al_2O_3 while the control gate is an N-type poly.

RESULTS AND DISCUSSION

Fig. 4 and 7 show programming and erase transient characteristics of the cells as described above. The combined use of the engineered tunnel barrier and Al_2O_3 IPD leads to a drastic decrease in the required programming voltage (9V programming and erase), as compared to memory cells with 8.5 nm SiO_2 tunnel dielectric and conventional ONO IPD (fig. 5 and 8) or industry-standard NAND memory cells [7] requiring 16V-19V.

Since Al_2O_3 has also been reported as charge trapping layer in MNOS-type memory cells [8], we have measured contacted floating gate memory cells (fig. 6 and 9) in order to assure that the observed memory effect in the floating gate cells is not due to charge trapping. As can be seen from these figures, applying either a positive or a negative bias to the device leads to a slight increase in threshold voltage, indicating electrons are being trapped in the Al_2O_3 layer (which is not surprising as the Variot stack is engineered for efficient electron injection at both

polarities), and it is not possible to use a negative gate voltage for detrapping these electrons, reducing the threshold voltage.

On floating gate memory cells (fig. 4 and 7), the V_{th} shift during programming is clearly larger than for the contacted floating gate memory cells, and the memory cells can be erased. Therefore, the memory operation is mostly due to charge in the floating gate and not (or only weakly in the programmed case) due to charge trapped in the Al_2O_3 layers.

The charge trapping in the Al_2O_3 layer limits the endurance, leading to a considerable shift and a reduction of the threshold voltage window after 200,000 write/erase cycles (fig. 10) although a large window can be maintained after 10,000 cycles. The charge that is trapped in the Al_2O_3 layer has a double effect on the endurance characteristic: on one hand, the intrinsic V_{th} (corresponding to the absence of charge on the floating gate) of the memory cell increases, thereby shifting the threshold voltage window upward. On the other hand, the electric field in the SiO_2 layers of the tunnel stack is reduced during programming and erase, therefore reducing the tunneling current and leading to a slight closure of the threshold voltage window.

The data retention of the Al_2O_3 -based memory cells is evaluated by performing temperature-accelerated measurements. Fig. 11 shows typical charge loss curves measured at 250°C for memory cells with different initial V_{th} windows. Particularly in the programmed condition, the V_{th} window size does not impact the (relative) charge loss at all, indicating that the leakage is not field-driven but purely temperature-driven. The extrapolation of data retention measurements performed at temperatures between 215°C and 300°C indicates that 10 years of data retention can be obtained up to a temperature of 120°C (fig. 12) for both the programmed and erased state.

CONCLUSIONS

We have demonstrated for the first time stacked gate memory cells with engineered tunnel barrier and Al_2O_3 interpoly dielectric. These cells can be programmed and erased by tunneling with a very low voltage and a reasonable endurance. Furthermore, we have demonstrated 10 years of data retention at 120°C for these memory cells, proving that Al_2O_3 is a suitable dielectric material for both tunnel and interpoly dielectric in floating gate Flash memory cells.

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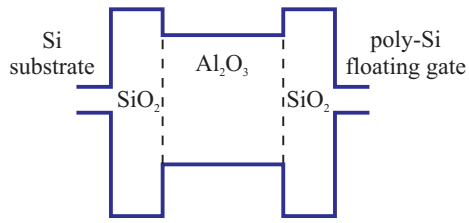


Figure 1: Band diagram of a $\text{SiO}_2/\text{Al}_2\text{O}_3/\text{SiO}_2$ triple-layer Variot stack with no applied bias. A low leakage can be achieved due to the thick stack.

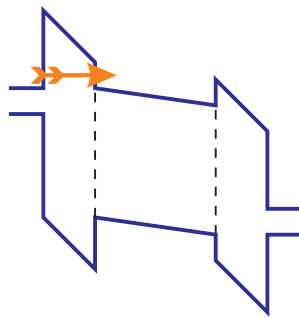


Figure 2: Band diagram of the same Variot stack when a moderate bias is applied. Due to the difference in dielectric constants, a high electric field is obtained in the SiO_2 layers for only a moderate total voltage across the stack. Furthermore, for a 2 nm SiO_2 bottom layer, the tunneling mechanism is direct tunneling, leading to a large tunneling current at moderate applied bias.

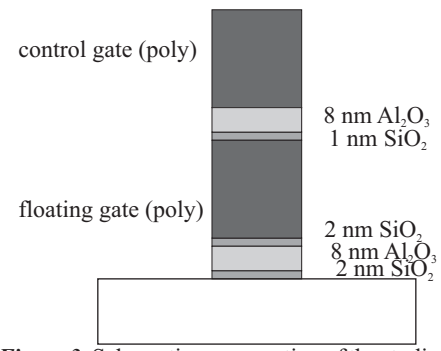


Figure 3: Schematic cross-section of the studied cell.

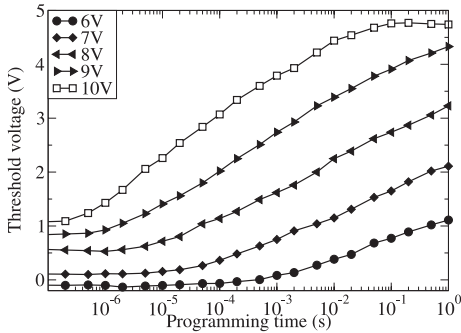


Figure 4: Programming transients of a 90 nm memory cell with 3-layer Variot tunnel dielectric and 8nm Al_2O_3 interpoly dielectric.

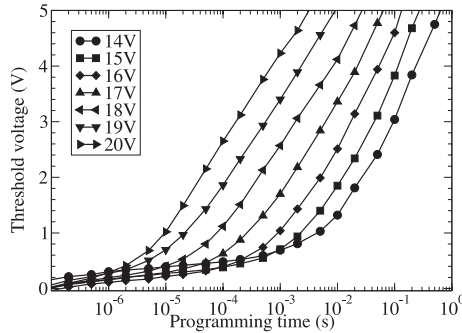


Figure 5: Programming transients of a 90 nm memory cell with an 8.5 nm SiO_2 tunnel dielectric and ONO interpoly dielectric.

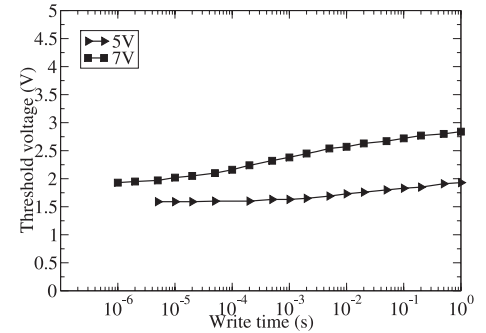


Figure 6: Programming transient on a contacted floating gate memory cell (therefore operated as a charge trapping device).

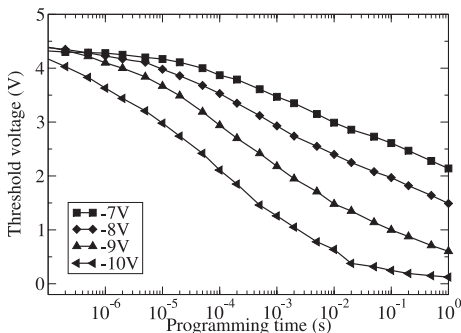


Figure 7: Erase transients of a 90 nm memory cell with 3-layer Variot tunnel dielectric and 8nm Al_2O_3 interpoly dielectric.

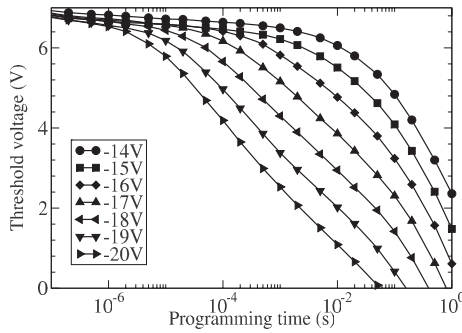


Figure 8: Erase transients of a 90 nm memory cell with 8.5 nm SiO_2 tunnel dielectric and ONO interpoly dielectric.

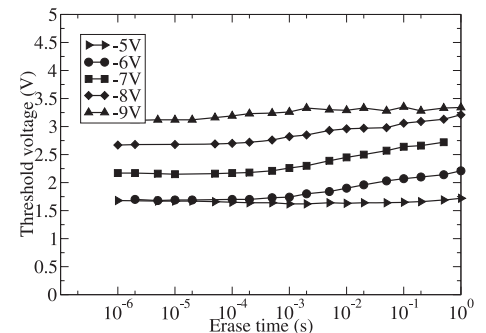


Figure 9: When negative pulses are applied to a contacted floating gate cell (charge trapping operation), it is impossible to decrease the threshold voltage. The different curves are measured successively on the same device.

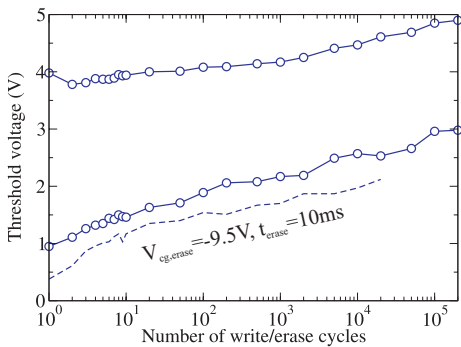


Figure 10: Cycling endurance using single-shot fixed conditions operation without verify after programming or erase. Programming is done with $V_{cg}=9\text{V}$, $t_{prog}=3\text{ms}$. Erasing is done with $V_{cg}=-9\text{V}$, $t_{crase}=3\text{ms}$.

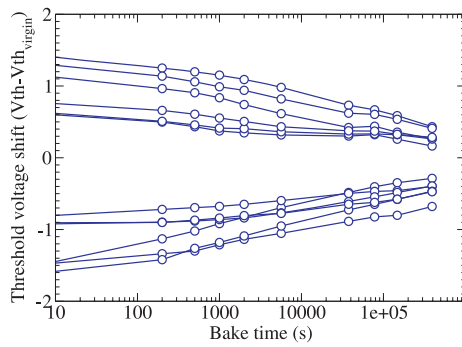


Figure 11: Data retention at 250°C of cells programmed and erased to different V_{th} . The virgin V_{th} is measured before the cell is subjected to program/erase operations, assuming that the post-metallisation anneal at 420°C is sufficient for fully erasing the cells.

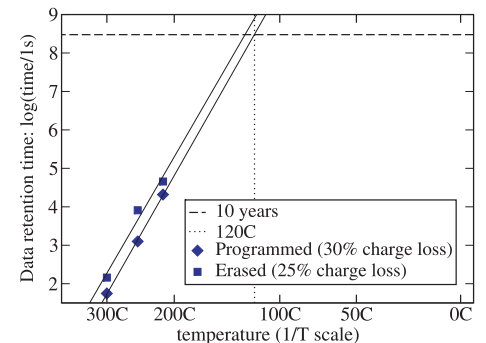


Figure 12: Temperature dependence of the data retention time. Assuming a $1/T$ behavior, 10 year retention is obtained up to 120°C . The charge loss is defined with respect to the virgin V_{th} .